EVAJIG

Turnkey PCBA testing & provisioning

EVAjig 1.0 Specifications

by

EVABITS

Revision history

DATE	DOCUMENT VERSION	CHANGES
4-10-2023	1.0	Initial document
17-10-2024	1.1	updated IOmodule specification v1.16

Contact information

Find more information on:
evabits.com
evajig.com
tel (EVAbits): +31 50 211 38 45

Disclaimer

Table of contents

EVAjig key specifications

The EVAjig programs and tests PCBAs using a bed of nails, targeted at cost efficiency of short production runs. The EVAjig provides a single platform, interface and backend which significantly reduces development time (for the end client), training and handling time (for the assembler), while providing state-of-the-art traceability. The low-cost, PCBA-specific cassettes have short production lead times and are interchangeable and can be replaced quickly and easily.

Key features

- Testbed for (functional) PCBA testing, programming and provisioning
- Generic platform enables a large number of tests out of the box
- Extensions possible for PCBA-specific test functionality
- Up to 12 DUTs per panel tested in parallel
- Cassettes are interchangeable and can be replaced in a matter of seconds; no tools required
- Cloud backend ensures full traceability of products, tests and test reports
- Short lead time and low-cost cassettes make this platform particularly suitable for short production runs
- Dispense with issues associated with testers built by clients, such as: training time, downtime by malfunctioning, maintenance and storage

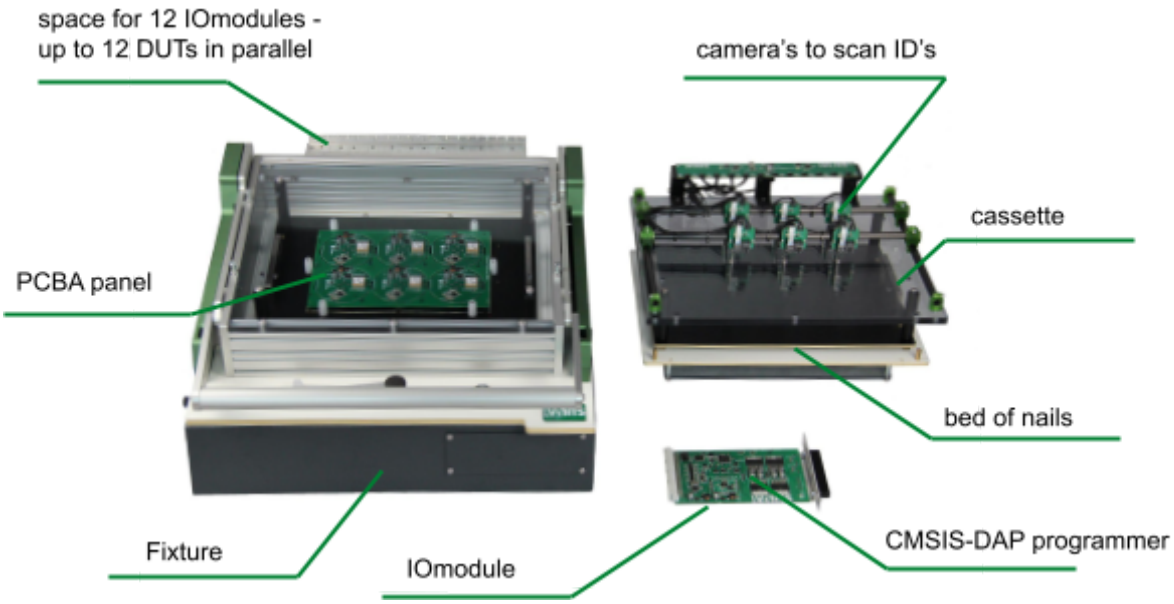
Benefits for the Client

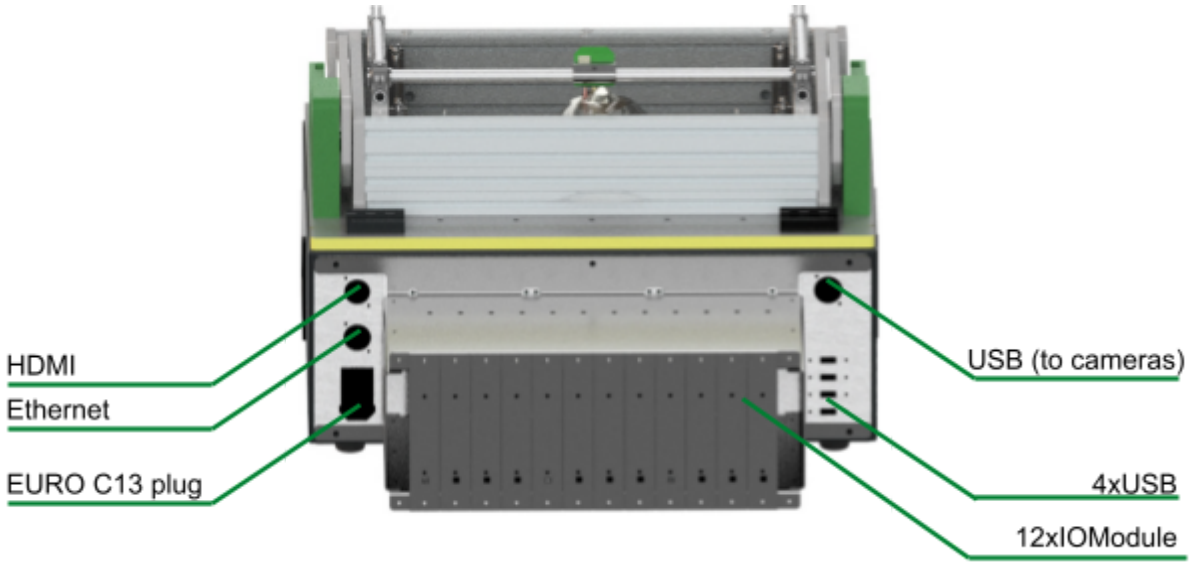
- Professional testing at low cost, thus effective for small series
- Less resources spent on production, so more can be spent on development
- Short lead times
- Many test capabilities provided out of the box
- Full traceability of products
- Hardware and software extensions can be made to integrate specific tests

Benefits for the Assembler

- Single platform for many PCBAs
    - Less time spent on training staff
    - Integration into company software
    - Less storage space
- Support by EVAbits
- Updates and upgradesIncrease customer value

System overview





Functional specifications

Fixture

- 12x IO module
- EURO C13 power plug
- 4x USB-A
- 1x USB-C (dedicated for the camera module)
- 1x HDMI
- 1x RJ45 / Ethernet
- Size (WxDxH): 470 x 680 x 330 [mm] (without cassette)
- Cassettes:
    - Generic PCB edge connector interface with 3x300 pins
    - Insertion lever
    - Protection against closing top when cassette is not inserted properly
- Operation:
    - Dedicated operator interface
    - Remote updates

Cassette

- DUT-specific placement of pogo pins, push fingers and cameras
- Generic PCB edge interface with 3x300 pins
- Recognition of cassette and test definition on insertion
- Maximum DUT size (WxD):
    - area with testpads: 290x200 [mm]
    - physical size: 300x220 [mm]
- Maximum height of components:
    - top side: 55 [mm]
    - bottom side:
        - < 3 [mm], no additional work required
        - 3 to 8 [mm], a window is milled into the top supporting plate
        - 8 to 40 [mm], a window is milled into both supporting plates
- Camera module:
    - Automated scanning of QR code or barcode stickers
    - Supports many formats
        - 2D:
            - QR Code, Data Matrix, PDF417, Code 128, Ean-13, Ean-8, UPC-E, UPC-A,
        - 1D:
            - ITF-25 (Interleaved 2 0f 5), Code39, Code93, Codabar
    - USB interface to fixture

IO module (v1.16)

- Power & Voltage:
  - 4x 12-bit adjustable voltage source between +/- 24V
  - software settable maximum current setting 0 to 4A
  - Power sources are shared with Analog Out (AO)
- Programming:
  - CMSIS-DAP adapter with SWD/JTAG, supporting many ARM-based and popular RISC-V-based processors, DSPs and FPGAs
  - Support for external JTAG
- Protocols:
  - UART, I2C, SPI,
  - RS232, RS485, Ethernet (require conversion to UART)
- Connectivity
  - Bluetooth, WIFI, LoRa
- Analog/Digital:
  - 18x DIO
    - at 1.8, 3.3 or 5V, settable in banks by a reference voltage pin
  - 8x AI between +/-24V
  - 4x AO between +/- 24V shared with power sources

Backend

- Portal for Electronics Manufacturing Service companies (EMSs)
  - Upload board/panel gerber files
  - Production run statistics
  - Access reports
- Portal for end clients
  - Upload gerbers
  - Upload binary or hex files
  - Create test definitions
  - Create work descriptions (operator views)
  - Access reports
- API
  - After test:
    - Direct access to data
  - In-test:
    - device provisioning
- Full traceability
  - Long-term storage of test definitions, binaries and reports

Operator Interface

- Adapts to cassette on insertion
- Detailed work instructions
- Various user levels
- Minimizes handling / clicking
- Export results by
    - network / USB printer
    - via portal:
        - JSON, CSV, PDF
    - cloud database API

Electrical specifications

EVAjig:

ITEM	VALUE	DESCRIPTION
power	240V, 5A (slow fuse)	EURO C13 cable
connectivity	1x HDMI 4x USB 1x Ethernet	Ethernet is highly recommended to access EVAjig backend
wireless	WIFI, BT(5.1)	Wireless is preferably only used for PCBA tests

IO module:

ITEM	VALUE	DESCRIPTION
power	+/-24V, 8A	
connectivity	1x USB-C 1x 96-pin (DIN 4162) 1x aux programming port	internal internal internal
4x PWR or Analog Out	voltage set -24V to 24V current limit 0 to 8A 12 bit	
1x 3.3V	1.0A fused	
1x 5.0V	1.0A fused	
1x JTAG (SWD)		voltage set internally
1x ETH	10/100Mbit	prolonged throughput is limited to 10Mbit
4x SERCOM	U(S)ART, or SPI, or I2C	Requires 2 to 4 DIO signals per SERCOM
18x Digital in/out	Static, PWM, FREQM	voltage set internally
4x Vref	1.2 to 5.0V	reference voltage for DIO
8x Analog in	-24V to 24V, 24bit, 100 ksps	

Mechanical specifications

EVAjig:

ITEM	VALUE	DESCRIPTION
dimensions (w/o cassette)	466x680x290	WxDxH, when closed
dimensions (w/ cassette, w/ camera module)	466x680x330	WxDxH, when closed

All dimensions in mm. A separate (touch)screen required for operation is not included.

Cassette:

ITEM	VALUE	DESCRIPTION
dimensions (w/o camera module)	373x330x127	WxDxH, when stored
dimensions (w/ camera module)	373x330x197	WxDxH, when stored

All dimensions in mm.

DUT and panel design guidelines

A production panel consists of one or more devices grouped together for the benefit of maximizing the efficiency of production machinery. There are several ways to construct panels. Usually though, there is a frame or breakaway around the panel of 5 to 10mm wide that gives structural support and ensures that components are some minimal distance from the panel edge.

	min	recommended	max	note
DUTs per panel	1	-	12	
Test pad diameter	1.00**	1.5	-	Use the largest diameter the design permits.
Test pad spacing (bottom)	1.27**	2.54	-	center to center
Test pad spacing (top)	1.27**	2.54	-	center to center, incurs additional costs
Panel size*	-	-	290 x 200	(WxD) area with testpads
	-	-	300 x 220	(WxD) max physical size
Alignment holes	2	-	-	Recommended to place 2 along panel edge diagonally opposite each other
Alignment hole diameter	3.00	-	3.20	

*Units are in mm unless noted otherwise. * Maximum panel sizes consider the standard sized fixture, contact EVAbits for PCBAs that require larger test areas. ** additional costs may be involved.*

The IO modules typically test a single DUT in a panel. For more complex DUTs that require more testpoints than a single IO module can offer, there's the option to have 2 or more IO modules handle a DUT. Standard PCBs are assumed to be 1.6mm thick.

DUT Identification

Fully automatic scanning of IDs using 1 camera per DUT.

2D

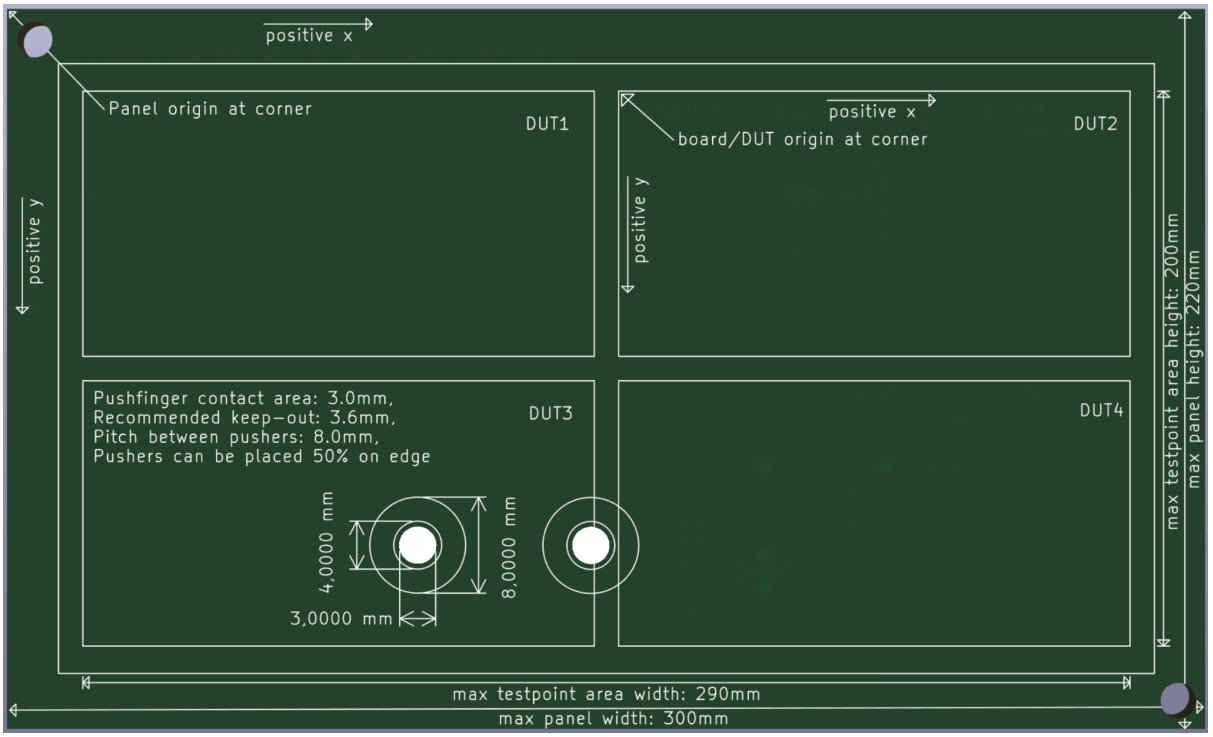
QR code	5.0x5.0 mm - 1024px		black on white stickers
Data Matrix	5.0x5.0 mm - 256 px		black on white stickers
Other			T.B.D. - Please contact us

For all scanning methods a maximum encoded data length of 255 bytes must be observed.
The identification (sticker) is assumed to be on the PCB surface.

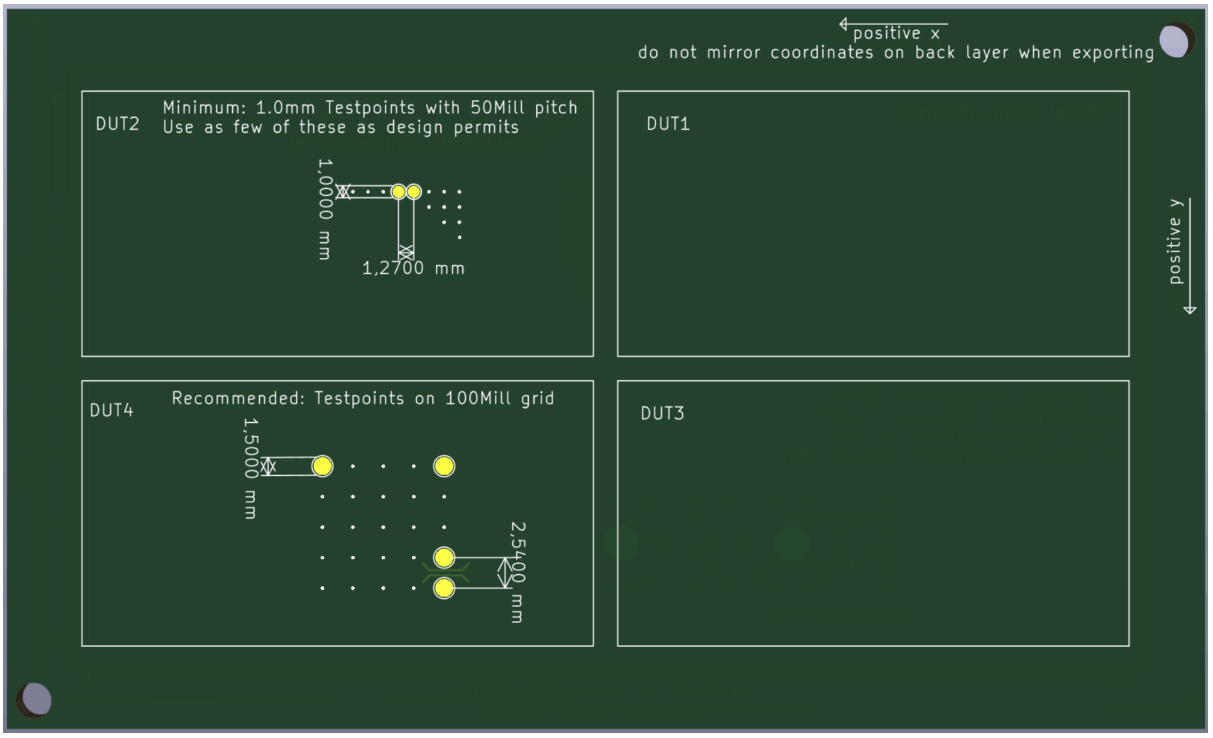
Hardware design recommendations

- Place all test pads on the bottom layer if your design permits it
- If there is not enough space for test pads, the panel frame can also be used
- Distribute the test points over the PCB area to distribute mechanical stress exerted by pogo pins.
- Ideally, the test pad locations are placed on a (2.54x2.54) grid.
- Inline test pads are preferred over endpoint pads (to prevent antenna effects). If that is not possible, make sure the trace length to the endpoint pad is as short as possible
- The pushfingers pressing the PCBA onto the pogo pins benefit from:
    - placement above a component-free area on the top side
    - placement close to (a cluster of) test pads
    - please consider an area of 3.6mm diameter or larger; the pushfinger contact/tip is 3.0mm in diameter.
    - the tip can be designed on the edge of a PCBA to about 50% coverage
- Place two alignment holes near the panel edge for precise alignment.
    - Two diagonally opposite corners, top-left and bottom-right, are recommended
- Components on the bottom side that are higher than 3.0mm require an additional cutout in the cassette
- Please contact EVAbits when components on the bottom side are higher than 8.0mm

The figures below show the parameters and recommendations on a panel.



Top.



Back.

Software and Test design recommendations

We recommend increasing the test coverage and test speed by programming firmware that is specialized for self-test wherever possible. The JTAG interface (RTT), a separate UART or another communication channel can be used to let the results be known to the EVAjig.

A few guidelines in order to successfully evaluate the self-test:

- Put concise information on any of the communication ports, indicating:
    - success
    - failure
    - no response within a specified time is also a failure
- Check every functionality individually and report back on each one to enable better fault-finding
- A single variable per line can be read and used in testing (UART) communication
    - make sure such a line can be uniquely found, for example:
        - “<unique identifier>: 3.33V\r\n”